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<b>PRE-APPEAL BRIEF REQUEST FOR REVIEW</b>		Docket Number (Optional)  SC12303EM																			
Certificate of Transmission under 37 CFR 1.8  I hereby certify that this correspondence is being _____ facsimile transmitted or <u>  X  </u> e-filed to the United States Patent and Trademark Office - Mail Stop AF.  on _____ <u>May 20, 2008</u> _____  Signature <u>  /Stacie Herrera/  </u> Typed or printed name: Stacie Herrera		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="2">Application Number</td> <td>Filed</td> </tr> <tr> <td colspan="2">10/531756</td> <td>04/14/2005</td> </tr> <tr> <td colspan="3">First Named Inventor</td> </tr> <tr> <td colspan="3">RAUBUCH, MARTIN</td> </tr> <tr> <td>Art Unit</td> <td colspan="2">Examiner</td> </tr> <tr> <td>2183</td> <td colspan="2">William B. Partridge</td> </tr> </table>		Application Number		Filed	10/531756		04/14/2005	First Named Inventor			RAUBUCH, MARTIN			Art Unit	Examiner		2183	William B. Partridge	
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<p>Applicant request review of the final rejection in the above identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s).          Note: No more than five (5) pages may be provided.</p> <p>I am the</p> <div style="display: flex; justify-content: space-between;"> <div style="width: 60%;"> <p><input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest.          See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.          (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record.          Registration number: 41,711</p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34          Registration number if acting under 37 CFR 1.34 _____</p> </div> <div style="width: 35%; text-align: center;"> <p>_____ /David G. Dolezal/ Signature</p> <p>_____ David G. Dolezal Typed or printed name</p> <p>_____ (512) 996-6839 Telephone number</p> <p>_____ May 20, 2008 Date</p> </div> </div> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.          Submit multiple forms if more than one signature is required, see below*.</p>																					

☒ \*Total of   1   forms are submitted

The collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality if governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S)	Martin Raubuch	GROUP ART UNIT: 2183
APPLN. NO.:	<b>10/531,756</b>	EXAMINER: William B. Partridge
FILED:	04/14/2005	DOCKET NUMBER: <b>SC12303EM</b>
ARRANGEMENT SYSTEM AND METHOD FOR VECTOR PERMUTATION IN SINGLE-INSTRUCTION MULTIPLE-DATA MICROPROCESSORS		

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Certificate of Submission

I hereby certify that this correspondence is being submitted to the U.S.P.T.O., Alexandria, VA.

- ☐ Addressed per C.F.R. § 1.1(a) and deposited with the United States Postal Service with sufficient postage as first class mail.
- ☐ Facsimile transmitted in accordance with C.F.R. § 1.6(d).
- ☐ Submitted electronically via EFS in accordance with "Legal Framework for EFS Web".

May 20, 2008

Date of Submission

/Stacie Herrera/

Signature

Stacie Herrera

Printed Name of Person Signing Certificate

STATEMENT OF REASONS FOR PRE-APPEAL BRIEF REVIEW

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Responsive to the Office Action dated February 20, 2008 (Final Office Action), please enter the following remarks in the above-entitled application, without prejudice or disclaimer.

**REMARKS**

Claims 1-10, 14-29 are pending.

A Request for Continued Examination was filed on May 17, 2007. A Non-Final Office Action dated July 26, 2007 followed the RCE and preceded the Final Office Action dated February 20, 2008.

Claims 1 – 7, 9, 14, 15, 17, 20 and 22 - 29 stand rejected under 35 USC § 103(a) as being obvious over US patent No. 5,996,057 (hereinafter referred to as "the Scales patent") in view of US patent No. 5,758,176 (hereinafter referred to as "the Agarwal patent").

Claim 1 recites an arrangement for vector permutation in a single-instruction multiple-data microprocessor. The arrangement comprises a vector register file and a permutation logic block, the permutation logic block being coupled to receive and permute vectors from at least one vector register of the vector register file according to control parameters. The permutation of the vectors is as a side operation of an instruction. A plurality of control

registers is also provided that is separate from the vector register file, each of the plurality of control registers being coupled to selectively provide control parameters to the permutation logic block. The arrangement also comprises a controller coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.

Claim 2 recites a single-instruction multiple-data microprocessor vector permutation system having analogous features to claim 1. Claim 5 recites a method for vector permutation in a single-instruction multiple-data microprocessor corresponding to the arrangement of claim 1.

Claim 28 recites an arrangement for vector permutation in a single-instruction multiple-data microprocessor analogous to claim 1, but with the further limitation of the controller also including at least one counter arranged to provide a sequential order for cyclically sequencing through the plurality of control registers.

For this Statement, Applicants will be focusing on four specific points:

- 1) The combined teachings of the Scales patent and the Agarwal patent fail to disclose that the permutation of the vectors is as a side operation of an instruction, as recited in Claims 1, 2 and 5;
- 2) The combined teachings of the Scales patent and the Agarwal patent fail to disclose that the control registers are provided to selectively provide control parameters to the permutation logic block, as recited in Claims 1, 2 and 5;
- 3) The skilled person would not be motivated to make the triple combination of the teachings of the Scales patent, the Agarwal patent and alleged Applicant Admitted Prior Art (AAPA); and
- 4) The Examiner overlooked the fact that the combination of the Scales patent and the Agarwal patent fail to teach the controller including at least one counter arranged to provide a sequential order for cyclically sequencing through the plurality of control registers, as recited in Claim 28.

1) The combined teachings of the Scales patent and the Agarwal patent fail to disclose that the permutation of the vectors is as a side operation of an instruction

The Final Office Action suggests that the combined teachings of the Scales patent and the Agarwal patent disclose the feature of the permutation of the vectors being as a side operation of an instruction. Applicants respectfully disagree.

The Scales patent relates to a data processing system (col. 2, line 59). According to col. 2, lines 60-66 of the Scales patent, the data processing system allows the specification of 3 input operands comprising 2 input vectors and a control vector. The input operands are loaded into vector registers and a Permute-With- Replication (PWR) operation is performed on the 2 input vectors in a manner specified by the control vector. The result of the PWR operation is stored as an output operand in an output register. The precise configuration of the data processing system disclosed in Scales patent is described further at col. 5, lines 31-48. In particular, col. 5, lines 33-34, the system comprises a vector register file 200 having 32 vector registers. The vector register file 200 is coupled to a combine network 210 (col. 5, lines 35-36). The vector register file 200 provide 3 vectors (A, B and C) from 3 pre-selected or programmed registers of the vector register file 200 (col. 5, lines 36-38). The PWR operation is

performed by the combine network 210, and the vector register file 200 includes a control register containing the control vector (col. 5, lines 46-47) does not disclose any relevant information relating to this feature.

The Final Office Action asserts that col. 2, line 59 – col. 3, line 13 and col. 4, line 49 – col. 6, lines 14 teach this feature, the latter cited passages being quite a lengthy passage. In any event, the Final Office Action alleges that the cited passages disclose that the vector PWR instruction does not directly cause the vector operation to occur, the vector PWR instruction only specifying which registers to use and the registers themselves cause the PWR operation to occur and cause the operation to replicate with interaction of another instruction. Again, Applicants respectfully disagree. Applicants' technical expert is very clear that the Scales patent does not disclose the feature of the permutation of the vectors as a side operation of an instruction. This is evidenced by the text of col. 5, lines 49 – 65, col. 6, line 52 – col. 7, line 40. Indeed, the Scales patent relates to high-performance, superscalar, processors (col. 3, lines 18 – 21) and so the need to perform side operations is antithetic in the context of such processors, because such processors can perform multiple instructions per cycle without the need for side-operations.

Furthermore, in the Response to Arguments section on pages 11 and 12 of the Final Office Action, the arguments advanced ignore the (above-recited) argument originally advanced at pages 2 and 3 of the Final Office Action. The Applicants thus conclude that the arguments set forth in the Response to Arguments section imply that the citation made on page 2 of the Final Office Action does not truly disclose the feature of the permutation of the vectors are as a side operation of an instruction.

Applicants therefore submit that the Scales patent does not disclose the feature of the permutation of the vectors being as a side operation of an instruction, as recited in Claims 1, 2 and 5.

Turning to the Agarwal patent, this document describes a single-instruction, multiple data (SIMD) execution unit for use in conjunction with a superscalar data processing system (Abstract). Referring to Figure 4 of the Agarwal patent, a superscalar processor 200 is interfaced with an SIMD execution unit 156. Referring to Figure 5, the SIMD execution unit 156 comprises a plurality of processing elements 230-234 coupled to a control unit 180 via a common command bus 184 and a plurality of individual data buses 186 (col. 7, lines 45-50). The processing elements 230-234 include a register file 236, the register file 236 optionally including 6 parts to allow a load or store operation to take place in parallel with an arithmetic operation. The register file 236 stores operands and results for vector operations performed by the processing elements 230-234 (col. 7, lines 51-57). Col. 8, lines 1-2 state that control registers 244 are included within the processing elements 233-234. Also, other control registers 244 may be used during operations that require indirect addressing of registers in the register file 236.

The final Office Action does not allege that the Agarwal patent discloses the feature of the side operation. Indeed, Applicants submit that the Agarwal patent does not disclose the feature of the permutation of the vectors being as a side operation of an instruction, as recited in Claims 1, 2 and 5.

Hence, neither the Scales patent nor the Agarwal patent disclose the feature of the permutation of the vectors being as a side operation of an instruction, as recited in claims 1, 2 and 5.

2) The combined teachings of the Scales patent and the Agarwal patent fail to disclose that the control registers are provided to selectively provide control parameters to the permutation logic block, as recited in Claims 1, 2 and 5

Page 5 of the Final Office Action states that while the Scales patent does not teach the plurality of control registers being provided as separate from the vector register file, the Agarwal patent discloses this feature. However, even if this feature is disclosed by the Agarwal patent, references in the Agarwal patent to “vectors” are in the context of vector computations. The Agarwal patent does not discuss the manipulation of the vectors, in particular permutation of the vectors. Consequently, it is submitted that even when the teachings of the Agarwal patent are combined with the Scales patent, the resulting combination still fails to teach that each of the plurality of control registers are coupled to selectively provide control parameters to the permutation logic block, as claimed in Claims 1, 2, and 5. In this respect, while the Agarwal patent discusses (col. 5, lines 37 – 38 and col. 8, lines 1 – 6) the control registers 244, the Agarwal patent does not disclose that the separate control registers are used for the performance of permutations. In this regard, the Agarwal patent is silent. It therefore follows that any combination made would be without direction as to what to do with the separate control registers of the Agarwal patent. To allege that the combination of the Scales and Agarwal patents disclose this additional feature therefore requires an unfounded presumption that is not disclosed in the cited documents (what to do with the registers) and so requires that application of hindsight.

Hence, the combination of the Scales patent and the Agarwal patent fails to disclose the feature of the plurality of control registers being coupled to selectively provide parameters to the permutation logic block, as recited in claims 1, 2 and 5.

3) The skilled person would not be motivated to make the triple combination of the teachings of the Scales patent, the Agarwal patent and alleged Applicant Admitted Prior Art (AAPA)

The Response to Arguments section of the Final Office Action states that the feature of the permutation of the vectors being as a side operation of an instruction is disclosed in the Applicants specification on page 4, lines 14 – 31. The Final Office Action therefore argues that the admitted prior art would be combined, by the skilled person, with the teachings of the Scales patent and the Agarwal patent.

Applicants respectfully disagree with this reasoning, because Applicants believe that the skilled person would not make the triple combination for the following reasons.

The Scales patent relates to superscalar (col. 3, lines 18 – 21) high-performance (col. 4, lines 53-56) processors. The Agarwal patent also relates to superscalar (for example, see title and col. 2, lines 42 – 46) high-performance processors. It should be appreciated that such high-performance processors are capable of multiple instructions per cycle. Therefore, there is no need to implement side-operations and so the skilled person would not be motivated to implement side operations in the architectures of the Scales patent and the Agarwal patent. Furthermore, the provision of side-operation capability serves to complicate an architecture of a high-performance processor resulting in performance penalties. The motivation for use of side-operations is to maximize use of a limited number of registers and hence minimize die space occupied by the processor. Such considerations are not relevant for non-embedded applications for which such high-performance processors are used.

It is therefore submitted that the skilled person would not strive to improve the processor of the Scales patent and the Agarwal patent by providing the performance of the permutations as side-operations of an instruction.

- 4) The Examiner overlooked the fact that the combination of the Scales patent and the Agarwal patent fail to teach features of claim 28

The Final Office Action states (at page 8, lines 10 – 12 thereof) that claims 28 and 29 contain the same limitations as claims 1 and 2 and are rejected for the same reasons set forth in connection with the rejections of claims 1 and 2. Applicants respectfully disagree.

Claim 28 contains different features to claim 1 and claim 2, namely the controller includes at least one counter arranged to provide a sequential order for cyclically sequencing through the plurality of control registers.

It is therefore submitted that the rejection of Claim 28 is improper. Furthermore, it is submitted that the Scales patent and the Agarwal patent, in any event, fail to disclose directly or inherently the feature of the controller including at least one counter arranged to provide a sequential order for cyclically sequencing through the plurality of control registers, as recited in Claim 28.

Respectfully submitted,

SEND CORRESPONDENCE TO:

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